MICRO LOGIC CORP.
μP CONSULTANTS

8080A & 8085A

MICROPROCESSOR INSTANT REFERENCE CARD

MICRO CHART

100% PLASTIC

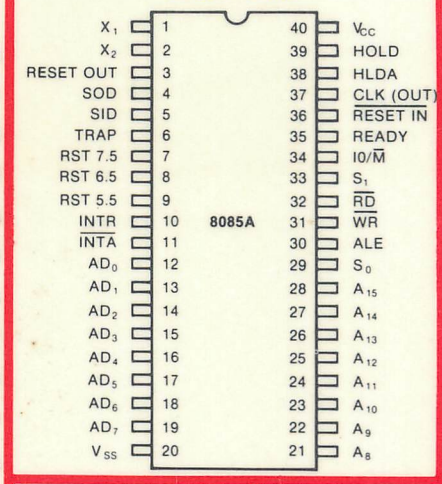
INSTANT ACCESS

HEX to Instruction Conversion

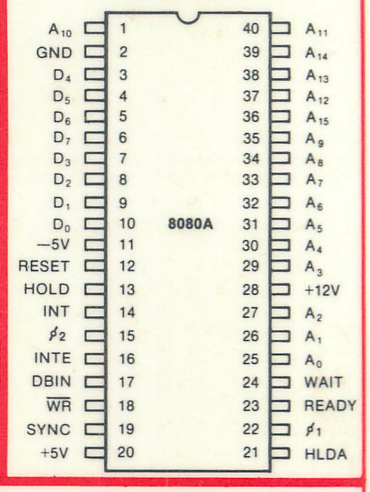
LSD →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	NOP	LXI B	STAX B	INX B	INR B	DCR B	MVI B	RLC	□	DAD B	LDAX B	DCX B	INR C	DCR C	MVI C	RRC	0
1	□	LXI D	STAX D	INX D	INR D	DCR D	MVI D	RAL	□	DAD D	LDAX D	DCX D	INR E	DCR E	MVI E	RAR	1
2	RIM	LXI H	SHLD	INX H	INR H	DCR H	MVI H	DAA	□	DAD H	LHLD	DCX H	INR L	DCR L	MVI L	CMA	2
3	SIM	LXI SP	STA	INX SP	INR M	DCR M	MVI M	STC	□	DAD SP	LDA	DCX SP	INR A	DCR A	MVI A	CMC	3
4	MOV B,B	MOV B,C	MOV B,D	MOV B,E	MOV B,H	MOV B,L	MOV B,M	MOV B,A	MOV C,B	MOV C,C	MOV C,D	MOV C,E	MOV C,H	MOV C,L	MOV C,M	MOV C,A	4
5	MOV D,B	MOV D,C	MOV D,D	MOV D,E	MOV D,H	MOV D,L	MOV D,M	MOV D,A	MOV E,B	MOV E,C	MOV E,D	MOV E,E	MOV E,H	MOV E,L	MOV E,M	MOV E,A	5
6	MOV H,B	MOV H,C	MOV H,D	MOV H,E	MOV H,H	MOV H,L	MOV H,M	MOV H,A	MOV L,B	MOV L,C	MOV L,D	MOV L,E	MOV L,H	MOV L,L	MOV L,M	MOV L,A	6
7	MOV M,B	MOV M,C	MOV M,D	MOV M,E	MOV M,H	MOV M,L	HLT	MOV M,A	MOV A,B	MOV A,C	MOV A,D	MOV A,E	MOV A,H	MOV A,L	MOV A,M	MOV A,A	7
8	ADD B	ADD C	ADD D	ADD E	ADD H	ADD L	ADD M	ADD A	ADC B	ADC C	ADC D	ADC E	ADC H	ADC L	ADC M	ADC A	8
9	SUB B	SUB C	SUB D	SUB E	SUB H	SUB L	SUB M	SUB A	SBB B	SBB C	SBB D	SBB E	SBB H	SBB L	SBB M	SBB A	9
A	ANA B	ANA C	ANA D	ANA E	ANA H	ANA L	ANA M	ANA A	XRA B	XRA C	XRA D	XRA E	XRA H	XRA L	XRA M	XRA A	A
B	ORA B	ORA C	ORA D	ORA E	ORA H	ORA L	ORA M	ORA A	CMP B	CMP C	CMP D	CMP E	CMP H	CMP L	CMP M	CMP A	B
C	RNZ	POP B	JNZ	JMP	CNZ	PUSH B	ADI	RST 0	RZ	RET	JZ	□	CZ	CALL	ACI	RST 1	C
D	RNC	POP D	JNC	OUT	CNC	PUSH D	SUI	RST 2	RC	□	JC	IN	CC	□	SBI	RST 3	D
E	RPO	POP H	JPO	XTHL	CPO	PUSH H	ANI	RST 4	RPE	PCHL	JPE	XCHG	CPE	□	XRI	RST 5	E
F	RP	POP PSW	JP	DI	CP	PUSH PSW	ORI	RST 6	RM	SPHL	JM	EI	CM	□	CPI	RST 7	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

8085A Pins



8080A Pins



Registers

A (Acc.)	(8)	Flags	(8)
B	(8)	C	(8)
D	(8)	E	(8)
H	(8)	L	(8)
PC (Program Counter)			(16)
SP (Stack Pointer)			(16)

Note: When BC, DE, HL used as pairs, B,D,H, are high order.

8085 Interrupts

Name	Adr	Type (starting with highest priority)
TRAP	24H	Rising edge & high level till sampled
RST 7.5	3CH	Rising edge (latched)
RST 6.5	34H	High level till sampled
RST 5.5	2CH	
INTR	− − −	

ASCII Character Set

LSD \ MSD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0 0000	NUL	DLE	SP	0	@	P	`	p
1 0001	SOH	DC1	!	1	A	Q	a	q
2 0010	STX	DC2	"	2	B	R	b	r
3 0011	ETX	DC3	#	3	C	S	c	s
4 0100	EOT	DC4	$	4	D	T	d	t
5 0101	ENQ	NAK	%	5	E	U	e	u
6 0110	ACK	SYN	&	6	F	V	f	v
7 0111	BEL	ETB	'	7	G	W	g	w
8 1000	BS	CAN	(	8	H	X	h	x
9 1001	HT	EM	)	9	I	Y	i	y
A 1010	LF	SUB	*	:	J	Z	j	z
B 1011	VT	ESC	+	;	K	[	k	{
C 1100	FF	FS	,	<	L	\	l	|
D 1101	CR	GS	-	=	M	]	m	}
E 1110	SO	RS	.	>	N	↑	n	~
F 1111	SI	US	/	?	O	←	o	DEL

Hex and Decimal Conversion

LSD →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	1
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	2
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	3
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	4
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	5
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	6
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	7
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	8
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	9
A	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	A
B	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	B
C	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	C
D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	D
E	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	E
F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Unsigned Comparisons

example: CMP B

A < B	JC YES
A ≤ B	JC YES ① JZ YES
A = B	JZ YES
A ≠ B	JNZ YES
A ≥ B	JNC YES
A > B	JC *+6 ① JNZ YES

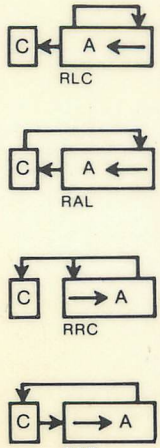
YES represents label for code to be executed if condition is true. Internally, A-B is computed to determine flags as for 'SUB B'.

① Requires both instructions.

8085A RIM & SIM bits

	MSB							LSB
RIM:	SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
SIM:	SOD	SOE	—	R7.5	MSE	M7.5	M6.5	M5.5

Rotate Instructions



Status Flags

MSB							LSB
S	Z	—	AC	—	P	—	C

S = sign (MSB) of result
Z = 1 = result is 0
AC = aux C from bit 3
P = 1 = parity is even
C = 1 = carry (also CY)

Miscellaneous

The 2 byte addresses in code, stack, and data areas are stored low byte followed by high byte. Thus, in hex, JMP 1234H is: C3 34 12.

SP points to used byte at top of stack. Stack push decrements SP by 2. High byte of pair is pushed first.

This card is based on specifications from Intel.®

8080 Timing Example

Using 8224 clock chip:

XTAL = 18 mhz/9 = 2 mhz
= 500 ns = 1 state.
ADD A = 4 states = 2 us

8085 Timing Example

XTAL = 6 mhz/2 = 3 mhz
= 333 ns = 1 state.
ADD A = 4 states = 1.333 us

DAA (Decimal Adjust Accumulator)

The 8 bits in the acc are adjusted to form 2 BCD digits by:

1. If the low 4 bits are > 9 or if the AC flag = 1, 6 is added to the acc.
2. If the high 4 bits are now > 9, or if CY = 1, 6 is added to the high 4 bits.

Flag Codes

Circled letters in Instruction Set indicate which flags are effected as follows:

- Ⓐ All
- Ⓑ All But C
- Ⓒ Just C
- Ⓓ Depends on which MPU:
  8080: All, C=0, AC=OR of bits 3
  8085: All, C=0, AC=1
- Ⓔ All, C=0, AC=0
- Ⓝ None

Abbreviations

- aa = a 2 byte address
- v = a 1 byte value
- vv = a 2 byte value
- M = Memory location that reg pair H&L points to
- S&F = States and Flag Codes
- LOC = Location
- MSE = Mask Set Enable
- PSW = Program Status Word (Acc & Flags)
- SID = Serial Input Data
- SOD = Serial Output Data
- SOE = Serial Output Enable

See also: "Registers" and "Status Flags"

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MICRO CHART

INSTRUCTION SET

	INSTRUCTION	OCT	HEX	S&F	DESCRIPTION
A	ADC A	217	8F	4	Double A with carry (shift left with carry)
	ADC B	210	88		Add B and carry to A
	ADC C	211	89		Add C and carry to A
	ADC D	212	8A		Add D and carry to A
	ADC E	213	8B		Add E and carry to A
	ADC H	214	8C		Add H and carry to A
	ADC L	215	8D	Ⓐ	Add L and carry to A
	ADC M	216	8E	7 Ⓐ	Add LOC (H&L) and carry to A
	ACI v	316	CE	7 Ⓐ	Add v and carry to A
	ADD A	207	87	4	Double A (shift A left)
	ADD B	200	80		Add B to A
	ADD C	201	81		Add C to A
	ADD D	202	82		Add D to A
	ADD E	203	83		Add E to A
	ADD H	204	84		Add H to A
	ADD L	205	85	Ⓐ	Add L to A
	ADD M	206	86	7 Ⓐ	Add LOC(H&L) to A
	ADI v	306	C6	7 Ⓐ	Add v to A
	ANA A	247	A7	4	Test A and clear carry
	ANA B	240	A0		AND B to A
	ANA C	241	A1		AND C to A
	ANA D	242	A2		AND D to A
	ANA E	243	A3		AND E to A
	ANA H	244	A4		AND H to A
	ANA L	245	A5	Ⓓ	AND L to A
	ANA M	246	A6	7 Ⓓ	AND LOC(H&L) to A
	ANI v	346	E6	7 Ⓓ	AND v to A
C	CALL aa	315	CD	17-18 Ⓝ	Call subroutine aa
	CZ aa	314	CC	11/17 - 9/18	If zero CALL
	CNZ aa	304	C4		If not zero CALL
	CP aa	364	F4		If plus CALL
	CM aa	374	FC		If minus CALL
	CC aa	334	DC		If carry CALL
	CNC aa	324	D4		If no carry CALL
	CPE aa	354	EC		If even parity CALL
	CPO aa	344	E4	Ⓝ	If odd parity CALL
	CMA	057	2F	4 Ⓝ	Complement A (1's comp)
	CMC	077	3F	4 Ⓒ	Complement carry
	CMP A	277	BF	4	Set zero flag
	CMP B	270	B8		Compare A with B
	CMP C	271	B9		Compare A with C
	CMP D	272	BA		Compare A with D
	CMP E	273	BB		Compare A with E
	CMP H	274	BC		Compare A with H
	CMP L	275	BD	Ⓐ	Compare A with L
	CMP M	276	BE	7 Ⓐ	Compare A with LOC(H&L)
	CPI v	376	FE	7 Ⓐ	Compare A with v
	DAA	047	27	4 Ⓐ	Decimal adjust A
D	DAD B	011	09	10	Add B&C to H&L
	DAD D	031	19		Add D&E to H&L
	DAD H	051	29		Double H&L (shift H&L left)
	DAD SP	071	39	Ⓒ	Add SP to H&L
	DCR A	075	3D	5-4	Decrement A
	DCR B	005	05		Decrement B
	DCR C	015	0D		Decrement C
	DCR D	025	15		Decrement D
	DCR E	035	1D		Decrement E
	DCR H	045	25		Decrement H
	DCR L	055	2D	Ⓑ	Decrement L
	DCR M	065	35	10 Ⓑ	Decrement LOC(H&L)
	DCX B	013	0B	5-6	Decrement B&C
	DCX D	033	1B		Decrement D&E
	DCX H	053	2B		Decrement H&L
	DCX SP	073	3B	Ⓝ	Decrement SP
E	DI	363	F3	4	Disable interrupts
	EI	373	FB	Ⓝ	Enable interrupts
H	HLT	166	76	7-5 Ⓝ	Halt until interrupt
I	IN v	333	DB	10 Ⓝ	Input from device v to A
	INR A	074	3C	5-4	Increment A
	INR B	004	04		Increment B
	INR C	014	0C		Increment C
	INR D	024	14		Increment D
	INR E	034	1C		Increment E
	INR H	044	24		Increment H
	INR L	054	2C	Ⓑ	Increment L
	INR M	064	34	10 Ⓑ	Increment LOC(H&L)
	INX B	003	03	5-6	Increment B&C
	INX D	023	13		Increment D&E
	INX H	043	23		Increment H&L
	INX SP	063	33	Ⓝ	Increment SP
J	JMP aa	303	C3	10 Ⓝ	Jump to LOC aa
	JZ aa	312	CA	10 - 7/10	If zero JMP
	JNZ aa	302	C2		If not zero JMP
	JP aa	362	F2		If plus JMP
	JM aa	372	FA		If minus JMP
	JC aa	332	DA		If carry JMP
	JNC aa	322	D2		If no carry JMP
	JPE aa	352	EA		If even parity JMP
	JPO aa	342	E2	Ⓝ	If odd parity JMP
L	LDA aa	072	3A	13 Ⓝ	Load A from LOC aa
	LDAX B	012	0A	7	Load A from LOC(B&C)
	LDAX D	032	1A	Ⓝ	Load A from LOC(D&E)
	LHLD aa	052	2A	16 Ⓝ	Load H&L from aa & next
	LXI B, vv	001	01	10	Load B&C with vv
	LXI D, vv	021	11		Load D&E with vv
	LXI H, vv	041	21		Load H&L with vv
	LXI SP,vv	061	31	Ⓝ	Load SP with vv
M	MOV A,B	170	78	5-4	Move B to A
	MOV A,C	171	79		Move C to A
	MOV A,D	172	7A		Move D to A
	MOV A,E	173	7B		Move E to A
	MOV A,H	174	7C		Move H to A
	MOV A,L	175	7D	Ⓝ	Move L to A
	MOV A,M	176	7E	7 Ⓝ	Move LOC(H&L) to A
	MOV B,A	107	47	5-4	Move A to B
	MOV B,C	101	41		Move C to B
	MOV B,D	102	42		Move D to B
	MOV B,E	103	43		Move E to B
	MOV B,H	104	44		Move H to B
	MOV B,L	105	45	Ⓝ	Move L to B
	MOV B,M	106	46	7 Ⓝ	Move LOC(H&L) to B
	MOV C,A	117	4F	5-4	Move A to C
	MOV C,B	110	48		Move B to C
	MOV C,D	112	4A		Move D to C
	MOV C,E	113	4B		Move E to C
	MOV C,H	114	4C		Move H to C
	MOV C,L	115	4D	Ⓝ	Move L to C
	MOV C,M	116	4E	7 Ⓝ	Move LOC(H&L) to C
	MOV D,A	127	57	5-4	Move A to D
	MOV D,B	120	50		Move B to D
	MOV D,C	121	51		Move C to D
	MOV D,E	123	53		Move E to D
	MOV D,H	124	54		Move H to D
	MOV D,L	125	55	Ⓝ	Move L to D
	MOV D,M	126	56	7 Ⓝ	Move LOC(H&L) to D
	MOV E,A	137	5F	5-4	Move A to E
	MOV E,B	130	58		Move B to E
	MOV E,C	131	59		Move C to E
	MOV E,D	132	5A		Move D to E
	MOV E,H	134	5C		Move H to E
	MOV E,L	135	5D	Ⓝ	Move L to E
	MOV E,M	136	5E	7 Ⓝ	Move LOC(H&L) to E
	MOV H,A	147	67	5-4	Move A to H
	MOV H,B	140	60		Move B to H
	MOV H,C	141	61		Move C to H
	MOV H,D	142	62		Move D to H
	MOV H,E	143	63		Move E to H
	MOV H,L	145	65	Ⓝ	Move L to H
	MOV H,M	146	66	7 Ⓝ	Move LOC(H&L) to H
	MOV L,A	157	6F	5-4	Move A to L
	MOV L,B	150	68		Move B to L
	MOV L,C	151	69		Move C to L
	MOV L,D	152	6A		Move D to L
	MOV L,E	153	6B		Move E to L
	MOV L,H	154	6C	Ⓝ	Move H to L
	MOV L,M	156	6E	7 Ⓝ	Move LOC(H&L) to L
	MOV M,A	167	77	7	Move A to LOC(H&L)
	MOV M,B	160	70		Move B to LOC(H&L)
	MOV M,C	161	71		Move C to LOC(H&L)
	MOV M,D	162	72		Move D to LOC(H&L)
	MOV M,E	163	73		Move E to LOC(H&L)
	MOV M,H	164	74		Move H to LOC(H&L)
	MOV M,L	165	75	Ⓝ	Move L to LOC(H&L)
	MVI A,v	076	3E	7	Move v to A
	MVI B,v	006	06		Move v to B
	MVI C,v	016	0E		Move v to C
	MVI D,v	026	16		Move v to D
	MVI E,v	036	1E		Move v to E
	MVI H,v	046	26		Move v to H
	MVI L,v	056	2E	Ⓝ	Move v to L
	MVI M,v	066	36	10 Ⓝ	Move v to LOC(H&L)
N	NOP	000	00	4 Ⓝ	No operation
O	ORA A	267	B7	4	Test A and clear carry
	ORA B	260	B0		OR B to A
	ORA C	261	B1		OR C to A
	ORA D	262	B2		OR D to A
	ORA E	263	B3		OR E to A
	ORA H	264	B4		OR H to A
	ORA L	265	B5	Ⓔ	OR L to A
	ORA M	266	B6	7 Ⓔ	OR LOC(H&L) to A
	ORI v	366	F6	7 Ⓔ	OR v to A
	OUT v	323	D3	10 Ⓝ	Output A to device v
P	PCHL	351	E9	5-6 Ⓝ	Jump to LOC(H&L)
	POP B	301	C1	10	Pop B&C from stack
	POP D	321	D1		Pop D&E from stack
	POP H	341	E1	Ⓝ	Pop H&L from stack
	POP PSW	361	F1	10 Ⓐ	Pop A and flags from stack
P	PUSH B	305	C5	11-12	Push B&C onto stack
	PUSH D	325	D5		Push D&E onto stack
	PUSH H	345	E5		Push H&L onto stack
	PUSH PSW	365	F5	Ⓝ	Push A and flags onto stack
R	RAL	027	17	4	Rotate CY & A left
	RAR	037	1F		Rotate CY & A right
	RLC	007	07		Rotate A left and into carry
	RRC	017	0F	Ⓒ	Rotate A right and into carry
	RIM (8085)	040	20	4 Ⓝ	Read interrupt mask
	RET	311	C9	10 Ⓝ	Return from subroutine
	RZ	310	C8	5-11 - 6-12	If zero RET
	RNZ	300	C0		If not zero RET
	RP	360	F0		If plus RET
	RM	370	F8		If minus RET
	RC	330	D8		If carry RET
	RNC	320	D0		If no carry RET
	RPE	350	E8		If even parity RET
	RPO	340	E0	Ⓝ	If odd parity RET
	RST 0	307	C7	11-12	Call subroutine at 00H
	RST 1	317	CF		Call subroutine at 08H
	RST 2	327	D7		Call subroutine at 10H
	RST 3	337	DF		Call subroutine at 18H
	RST 4	347	E7		Call subroutine at 20H
	RST 5	357	EF		Call subroutine at 28H
	RST 6	367	F7		Call subroutine at 30H
	RST 7	377	FF	Ⓝ	Call subroutine at 38H
S	SBB A	237	9F	4	Set A to minus carry
	SBB B	230	98		Subtract B & CY from A
	SBB C	231	99		Subtract C & CY from A
	SBB D	232	9A		Subtract D & CY from A
	SBB E	233	9B		Subtract E & CY from A
	SBB H	234	9C		Subtract H & CY from A
	SBB L	235	9D	Ⓐ	Subtract L & CY from A
	SBB M	236	9E	7 Ⓐ	Subtract LOC (H&L) & CY from A
	SBI v	336	DE	7 Ⓐ	Subtract v and CY from A
	SHLD aa	042	22	16 Ⓝ	Store H&L at aa & next
	SIM (8085)	060	30	4 Ⓝ	Set interrupt mask
	SPHL	371	F9	5-6 Ⓝ	Load SP from H&L
	STA aa	062	32	13 Ⓝ	Store A at LOC aa
	STAX B	002	02	7	Store A at LOC(B&C)
	STAX D	022	12	Ⓝ	Store A at LOC(D&E)
	STC	067	37	4 Ⓒ	Set carry (to 1)
	SUB A	227	97	4	Clear A
	SUB B	220	90		Subtract B from A
	SUB C	221	91		Subtract C from A
	SUB D	222	92		Subtract D from A
	SUB E	223	93		Subtract E from A
	SUB H	224	94		Subtract H from A
	SUB L	225	95	Ⓐ	Subtract L from A
	SUB M	226	96	7 Ⓐ	Subtract LOC(H&L) from A
	SUI v	326	D6	7 Ⓐ	Subtract v from A
X	XCHG	353	EB	4 Ⓝ	Exchange D&E with H&L
	XRA A	257	AF	4	Clear A
	XRA B	250	A8		Exclusive OR B to A
	XRA C	251	A9		Exclusive OR C to A
	XRA D	252	AA		Exclusive OR D to A
	XRA E	253	AB		Exclusive OR E to A
	XRA H	254	AC		Exclusive OR H to A
	XRA L	255	AD	Ⓔ	Exclusive OR L to A
	XRA M	256	AE	7 Ⓔ	Exclusive OR LOC (H&L) to A
	XRI v	356	EE	7 Ⓔ	Exclusive OR v to A
	XTHL	343	E3	18-16 Ⓝ	Exchange top of stack with H&L

EXAMPLES FROM S & F COLUMN

7	7 STATES FOR 8080 & 8085
5-4	5 STATES 8080; 4 STATES 8085
10-7/10	10 STATES 8080; 7 STATES FOR FAILURE, 10 STATES FOR SUCCESS ON 8085

DO NOT PLACE ON HOT SURFACES

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